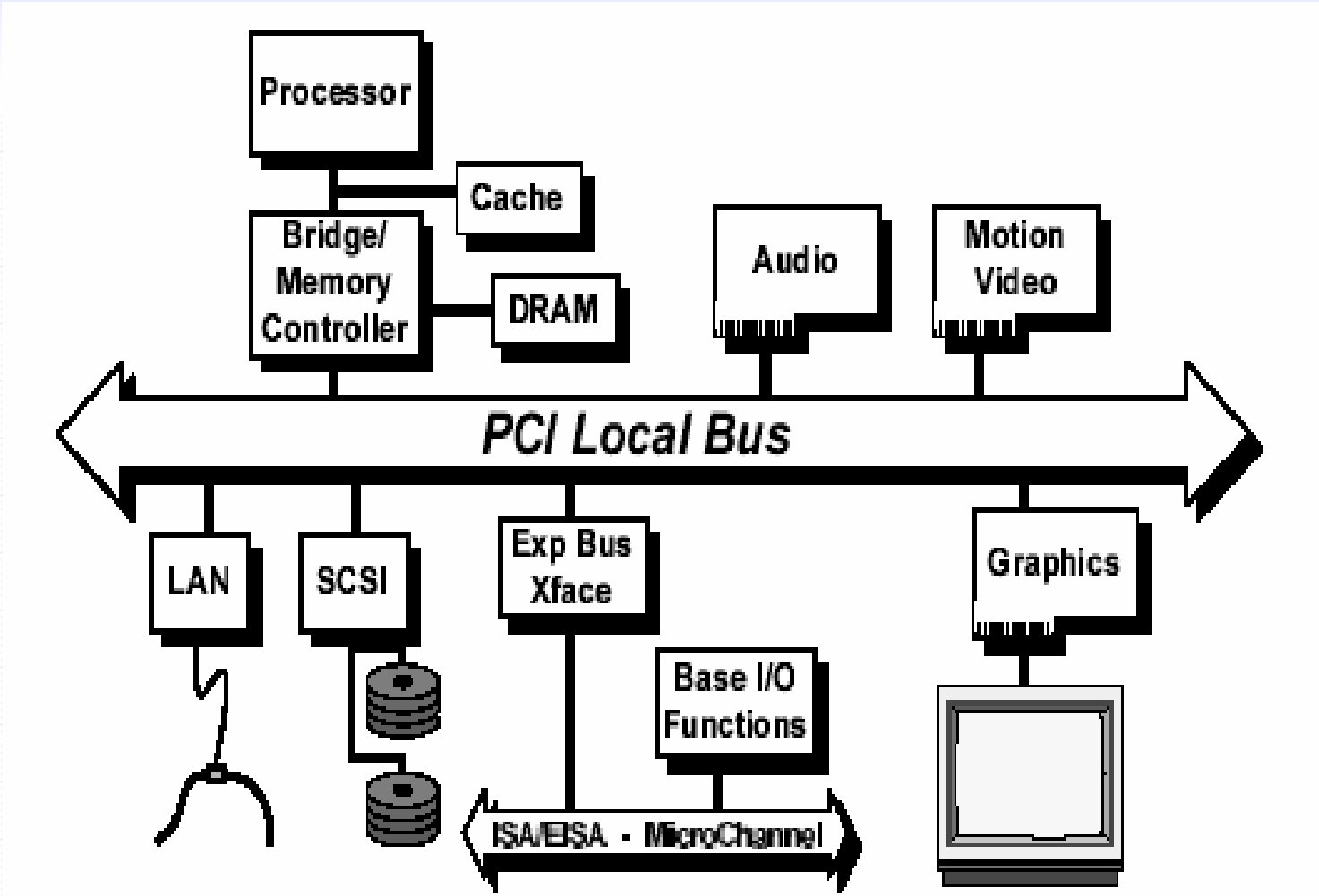
Advanced Computer Architecture

Lecture 13: PCI Local Bus

PCI Local Bus

PCI local bus is used for the expansion of computer systems by expansion bus add-in cards. PCI local bus acts as an interconnect mechanism between peripheral controller components and processor.

PCI Local Bus Architecture



PCI Bus Agents

(PCI is a Multimaster Bus)

Initiator (or Master)

Owns the bus and initiates the data transfer

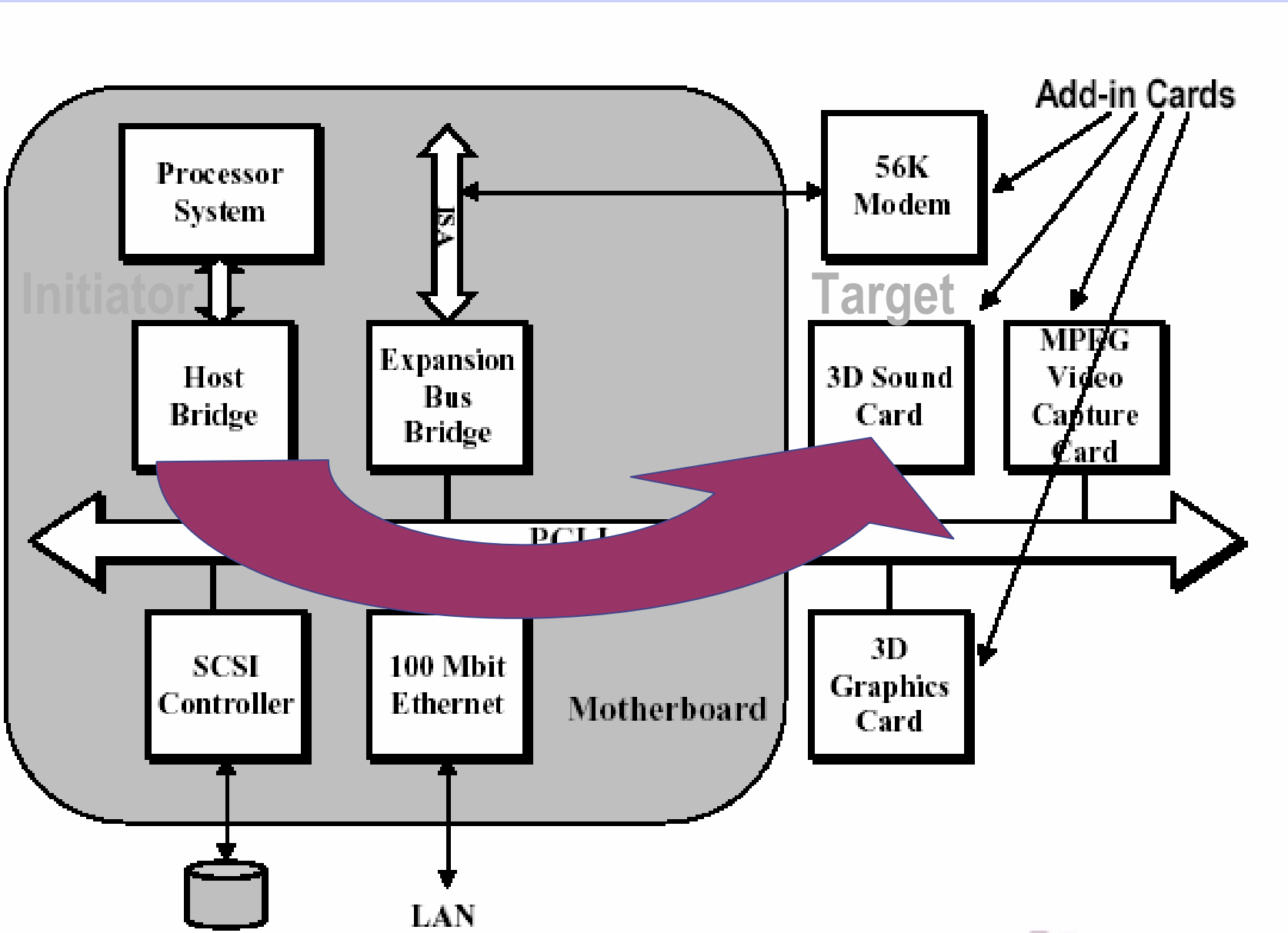
Target (or Slave)

Target of the data transfer (read or write)

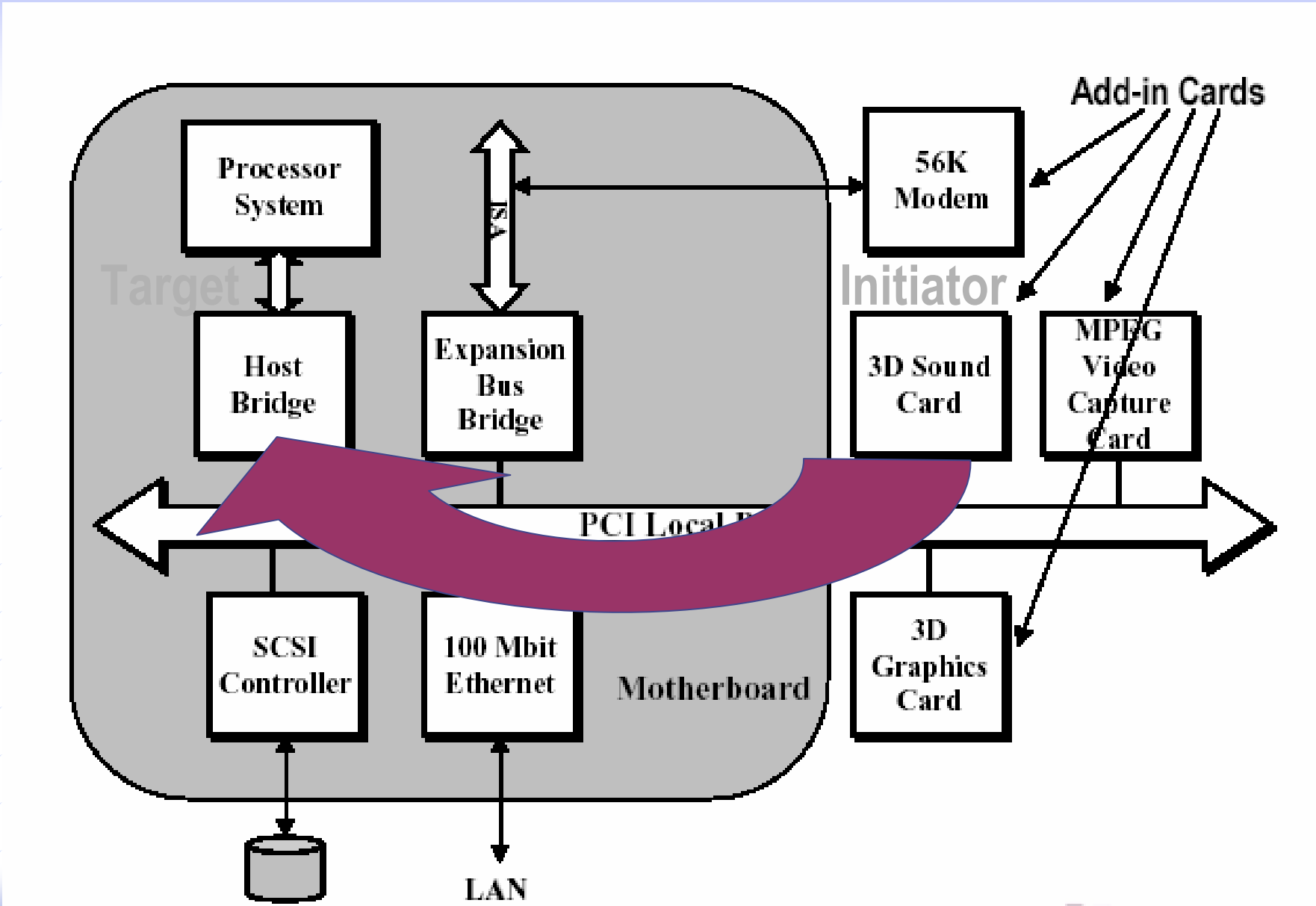
Agent

Any initiator/target or target on the PCI bus

Transaction from the Processor to Sound card



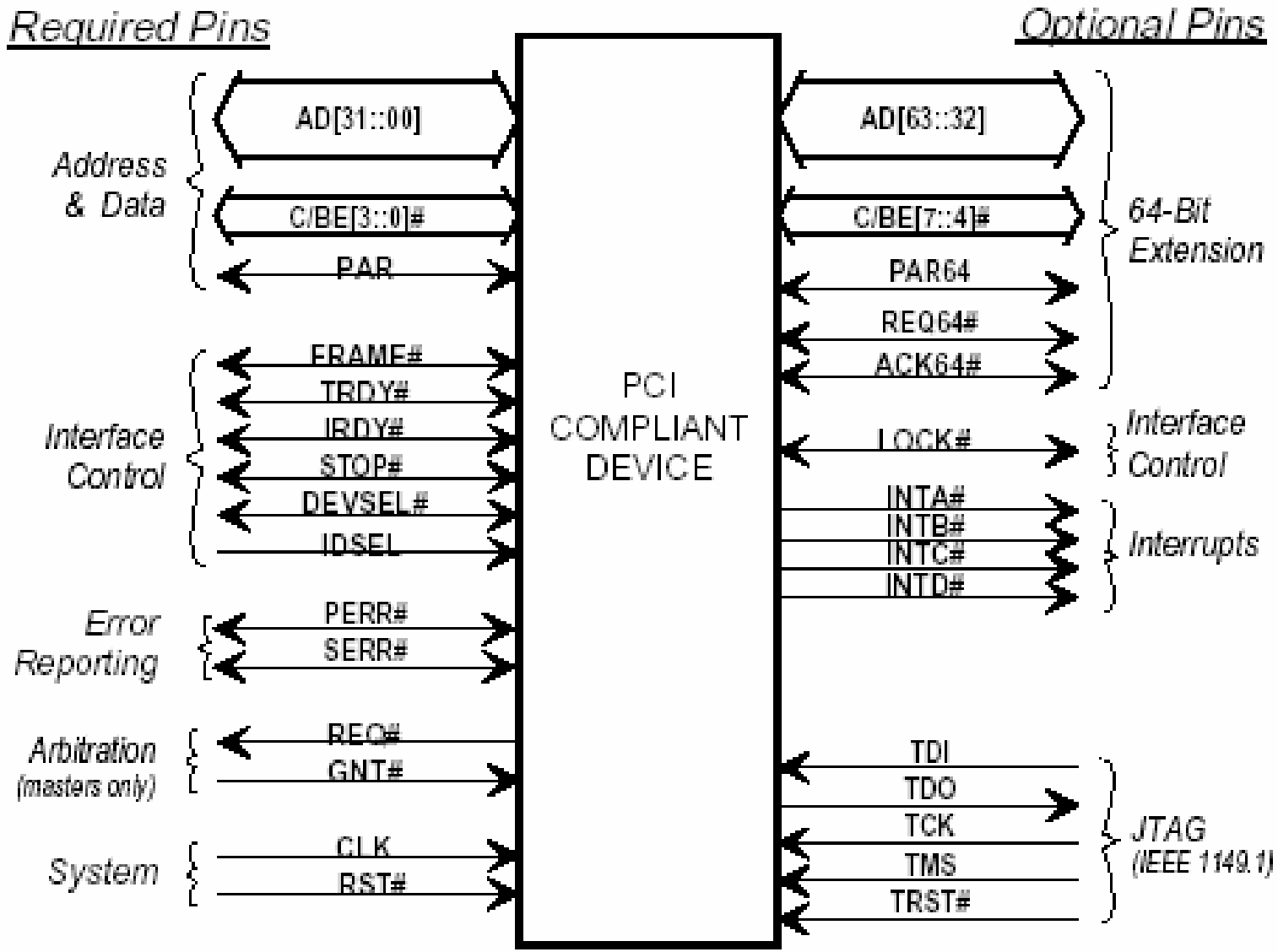
Transaction from the Sound card to Processor



PCI Fundamentals and Concepts

- PCI Local Bus Architecture
- PCI Signals
- Basic Bus Operations
- PCI Addressing and Bus Commands
- PCI Configuration spac and configuration accesses
- PCI Local Bus Arbiteration scheme
- PCI Bridges
- PCI-X

PCI Bus Signals



System Pins

- **Clk**

  PCI operates at 33 or 66 M Hz

- **Reset**

  Asynchronous reset Brings all the PCI specific signals to a consistant state

Address and Data Signals

- **AD[31:0] – I/O**
  - — Address and data are both multiplexed on the same PCI pins
  - — PCI supports both single and burst read and write transactions
- **C/BE#[3:0] – I/O**
  - — 4-bit command/byte enable bus
  - — Defines the PCI command during address phase
  - — Indicates byte enable during data phases
- **PAR – I/O**
  - — Parity bit
  - — Used to verify correct transmittal of address/data and command/byte-enable

Arbitration Signals

- (For initiators only)

Point-to-point connection to arbiter – each initiator has its own REQ# and GNT# line.

- REQ# O
  - Asserted by initiator to request bus ownership
- GNT# I
  - Asserted by system arbiter to grant bus ownership to the initiator

Transaction Control

- (Initiator signals)

- FRAME# I/O
  - Driven by the initiator to indicate the start and end of a transaction
- IRDY# I/O
  - initiator ready signal indicates that it is ready to send or receive data

Transaction Control

- (Target signals)
- TRDY# I/O
  - When the target asserts this signal, it tells the initiator that it is ready to send or receive data
- STOP# I/O
  - Used by target to indicate that it needs to terminate the transaction
- DEVSEL# I/O
  - Device select
  - Each target is responsible for decoding the address associated with each transaction
  - When a target recognizes its address, it asserts DEVSEL# to claim the corresponding transaction

Error Signals

- PERR# I/O
  - Indicates that a data parity error has occurred
- SERR# I/O
  - Indicates a serious system error has occurred
  - Example: Address parity error

PCI Transactions

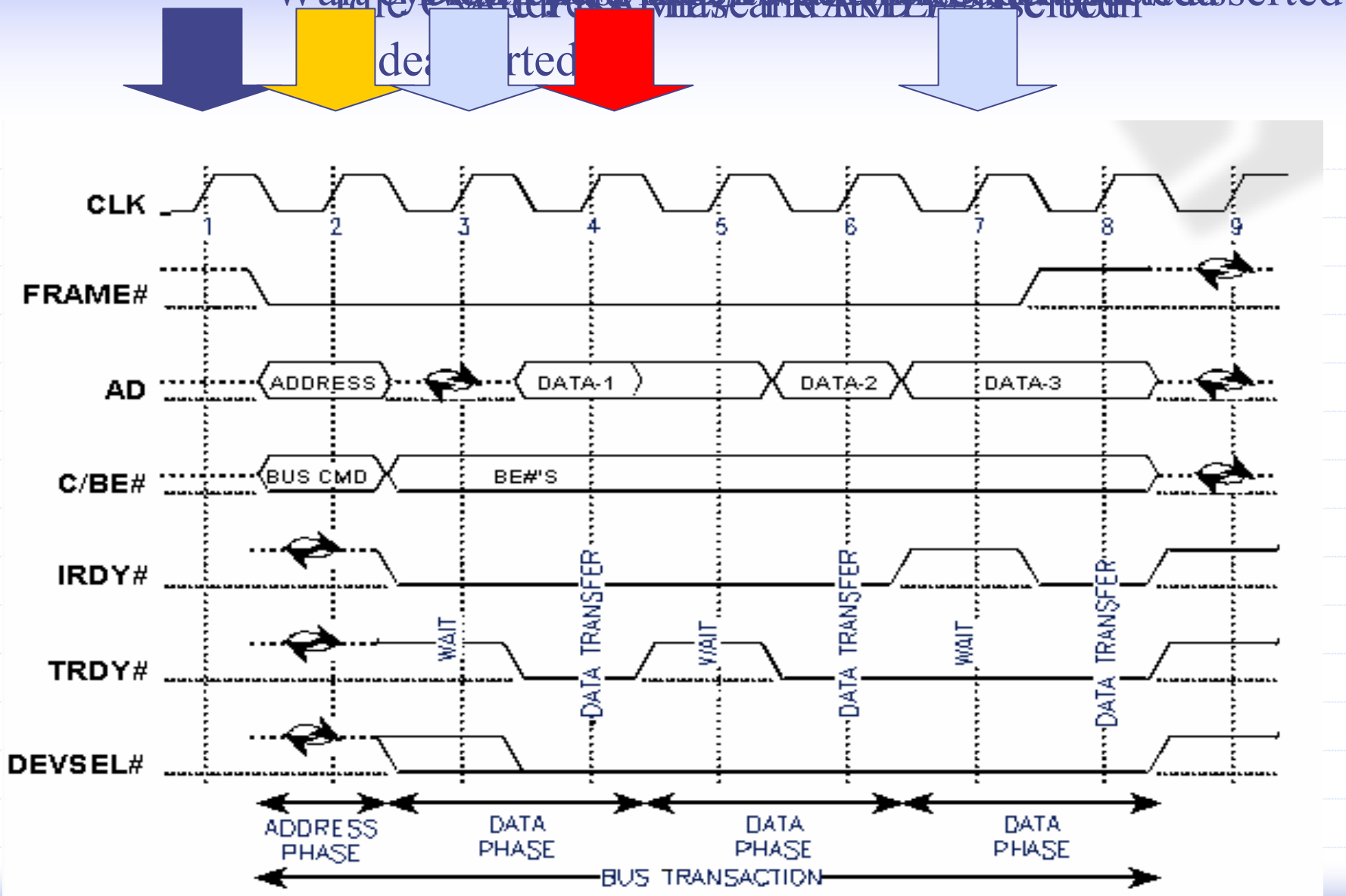
- A normal PCI transaction consists of one address phase followed by one or more data phases.

- Address Phase
  - Address Phase is the first cycle in which FRAME is asserted.
- Data Phase
  - Data Phase is the cycle in which both Irdy and Trdy are asserted

Terminologies

- **Idle cycle**
  - The cycle in which FRAME# and IRDY# are both deasserted.
- **Wait cycle**
  - If Irdy is asserted and Trdy deasserted or vise versa we have a wait cycle
  - Target deasserts TRDY# to signal it is not ready or Initiator deasserts IRDY# to signal it is not ready
- **Burst transaction**
  - Any transaction consisting of more than one data phases

PCI Bus Read


CLK
FRAME#
AD
C/BE#
IRDY#
TRDY#
DEVSEL#
1
2
3
4
5
6
7
8
9
ADDRESS
DATA-1
DATA-2
DATA-3
BUS CMD
BE#'S
WAIT
DATA TRANSFER
WAIT
DATA TRANSFER
WAIT
DATA TRANSFER
ADDRESS PHASE
DATA PHASE
DATA PHASE
DATA PHASE
BUS TRANSACTION

PCI Commands

- During the address phase of a transaction C/BE[3::0] defines the bus command.

	C/BE#	Command
	0000	Interrupt Acknowledge
	0001	Special Cycle
	0010	I/O Read
	0011	I/O Write
	0100	Reserved
	0101	Reserved
	0110	Memory Read
	0111	Memory Write
	1000	Reserved
	1001	Reserved
With IDSEL	1010	Configuration Read
With IDSEL	1011	Configuration Write
	1100	Memory Read Multiple
	1101	Dual Address Cycle
	1110	Memory Read Line
	1111	Memory Write and Invalidate

Memory

I/O

Configuration

Special-Purpose

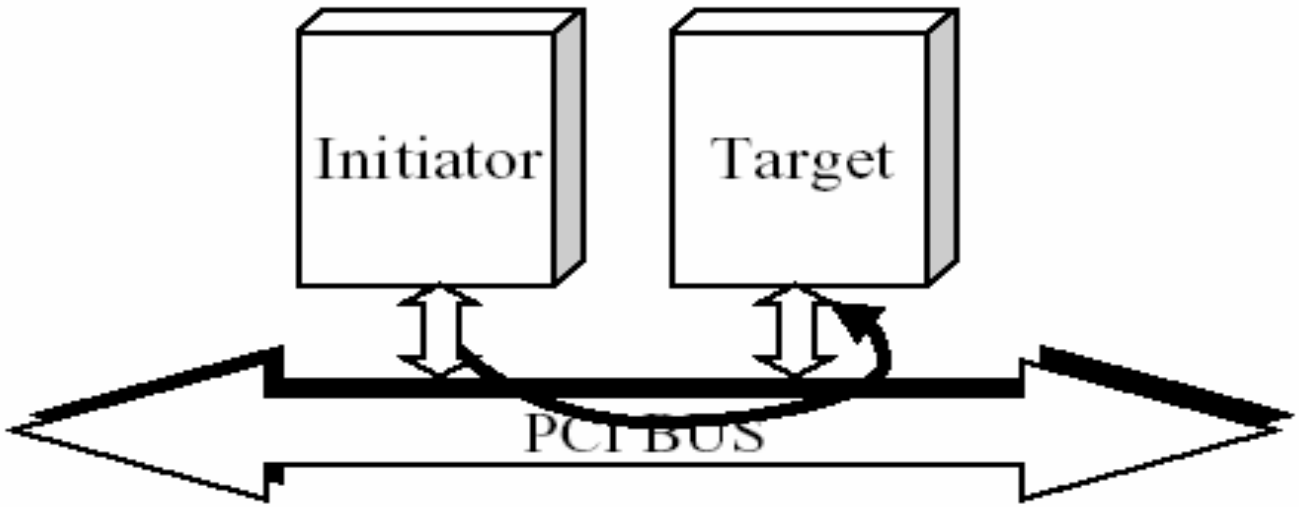
Reserved

Memory commands

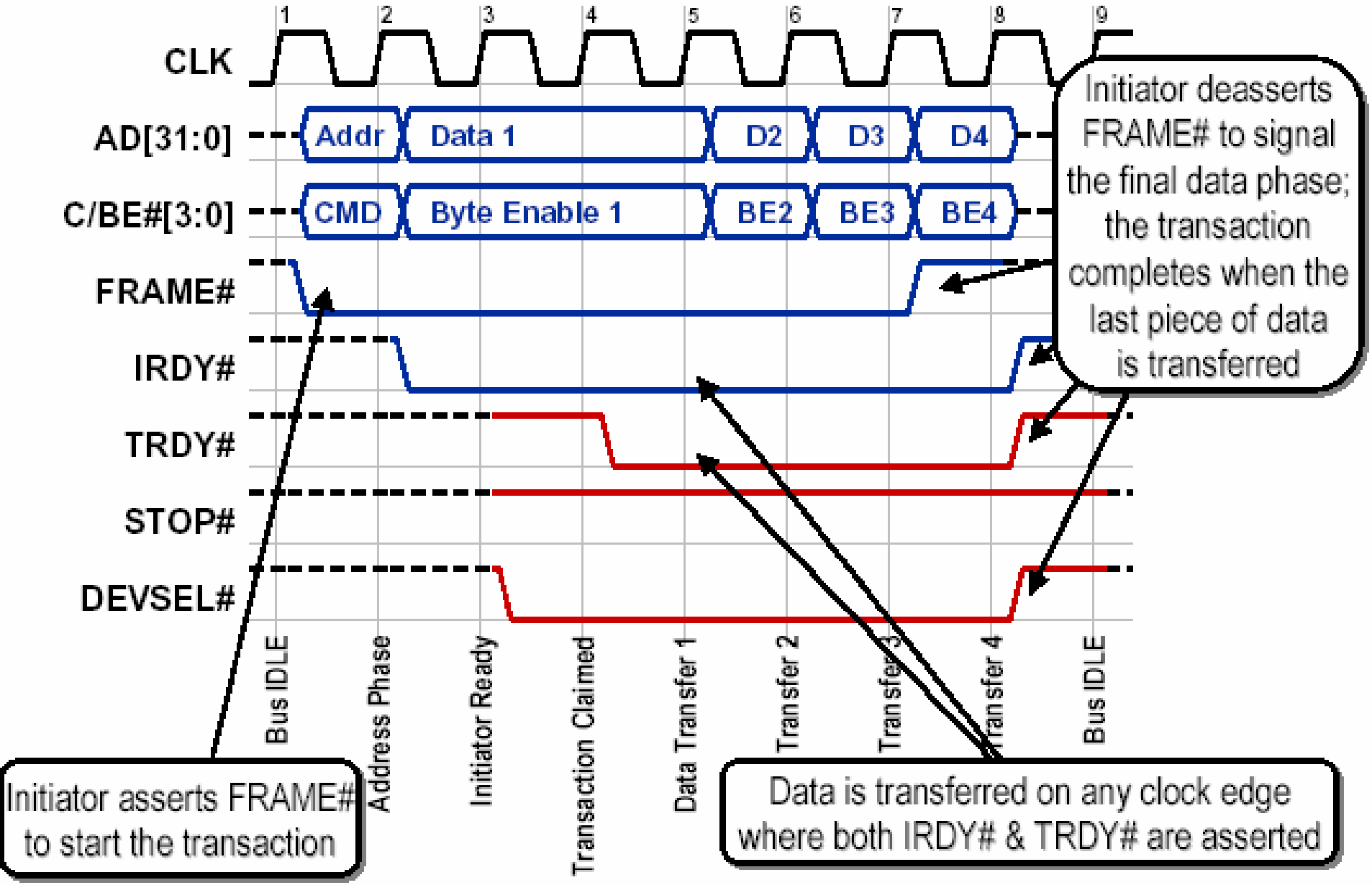
- Memory Write (0111)
  - Writes data to an agent mapped in memory address space
- Memory Write and Invalidate (1111)
  - Transfers a complete cacheline to memory, then invalidates the line in cache
  - Differs from Memory Write by its guarantee of a minimum transfer of one complete cacheline

Example : Memory Write

- A four-DWORD (32-bits) burst from an initiator to a target



Basic Write Transaction

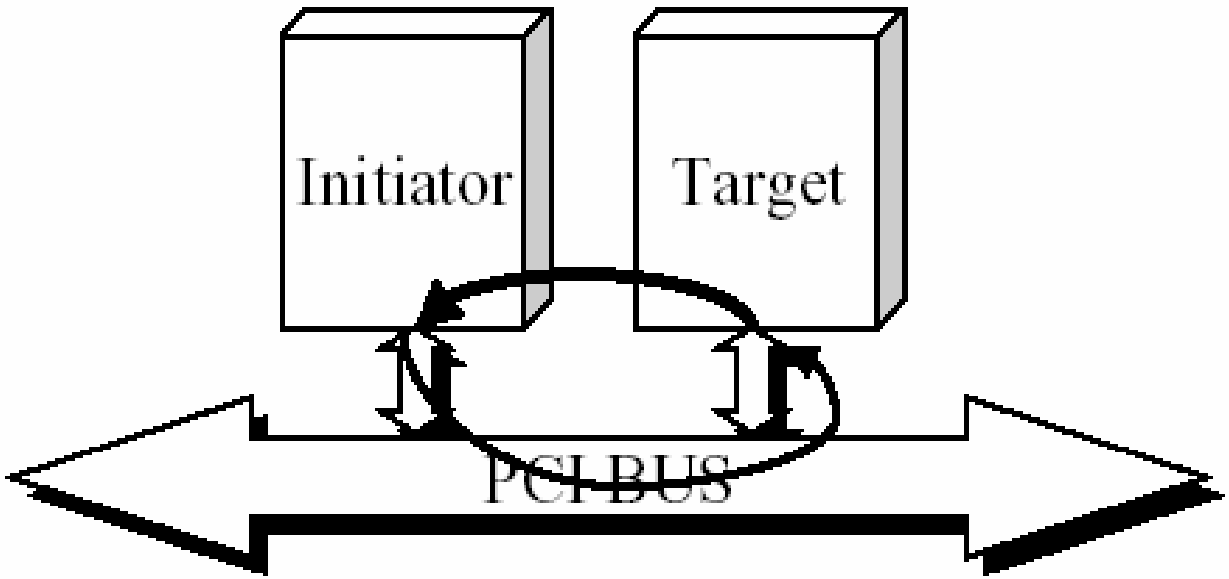


Memory commands

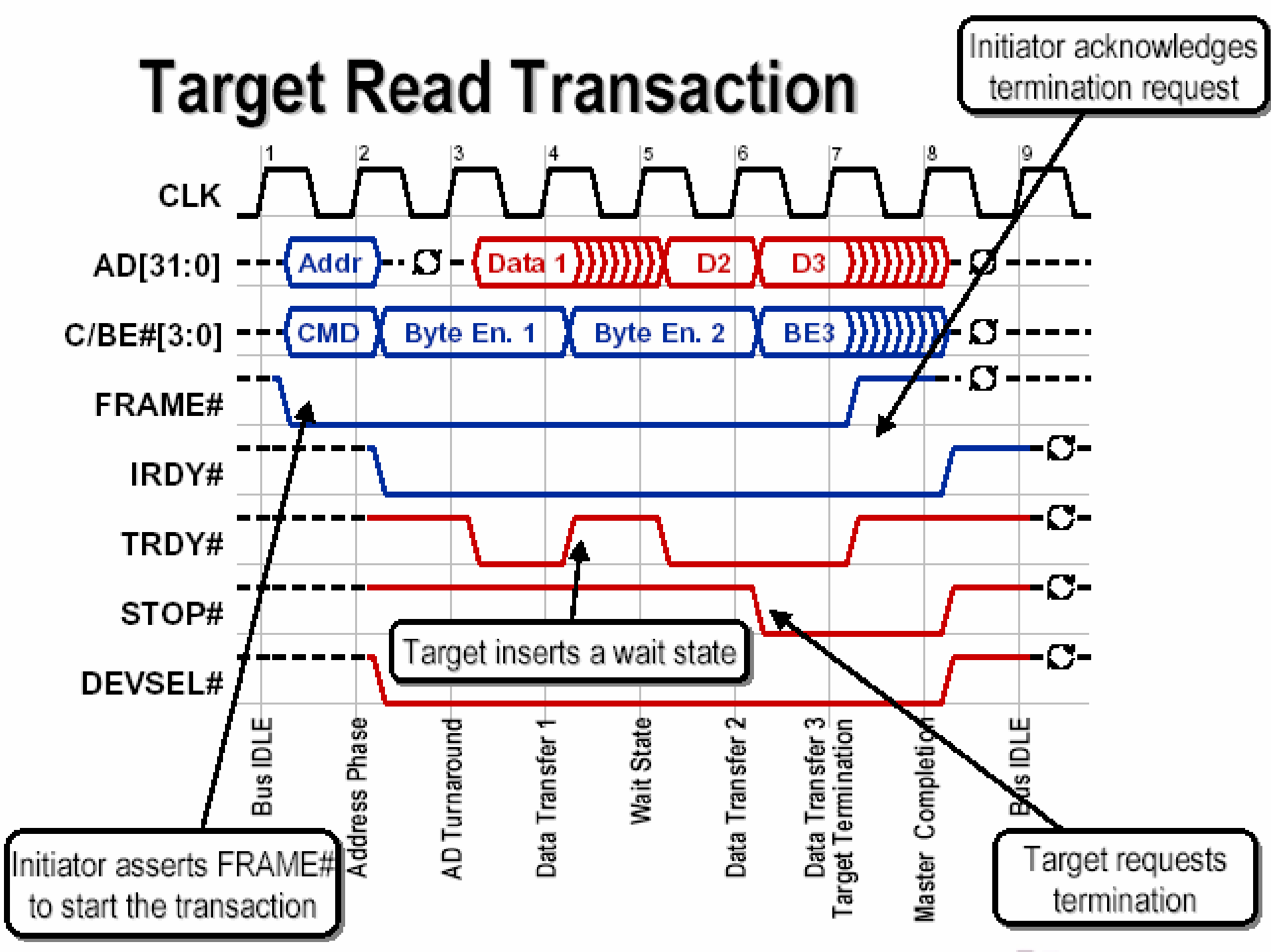
- Memory Read (0110)
  - Reads data from an agent mapped in memory address space
  - Target can do anticipatory read if no side effects can be guaranteed
- Memory Read Line (1110)
  - Reads up to the cacheline boundary
- Memory Read Multiple (1100)
  - Fetches a full cache line and starts fetching the next

Example : Memory read

A four-DWORD (32-bits) burst read from a target by an initiator



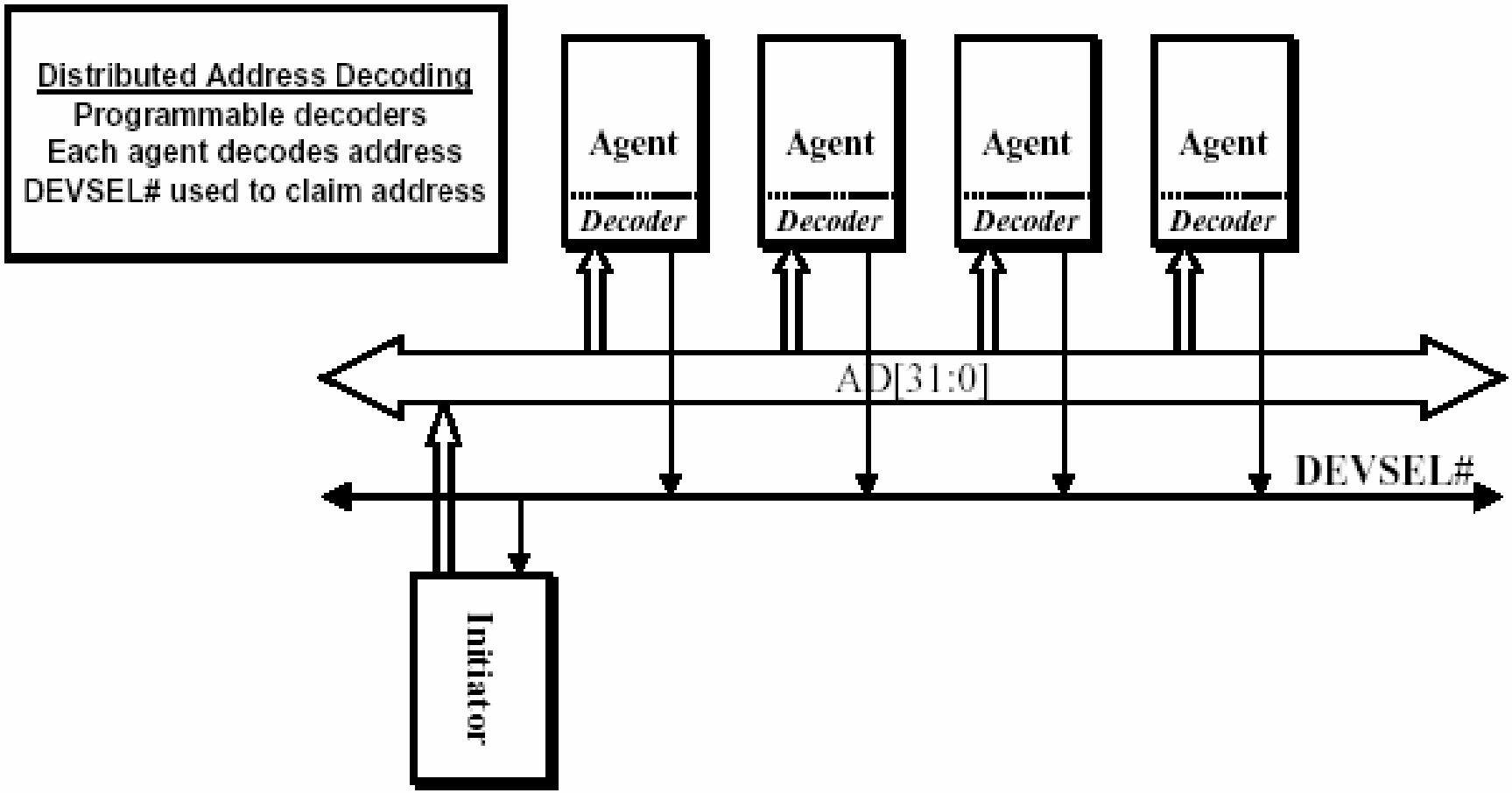
Target Read Transaction



Target Address Decoding

- PCI uses distributed address decoding
  - A transaction begins over the PCI bus
  - Each potential target on the bus decodes the transaction's PCI address to determine whether the transaction is meant for it or not
  - The target that owns the PCI address then claims the transaction by asserting DEVSEL#

Distributed Address Decoding



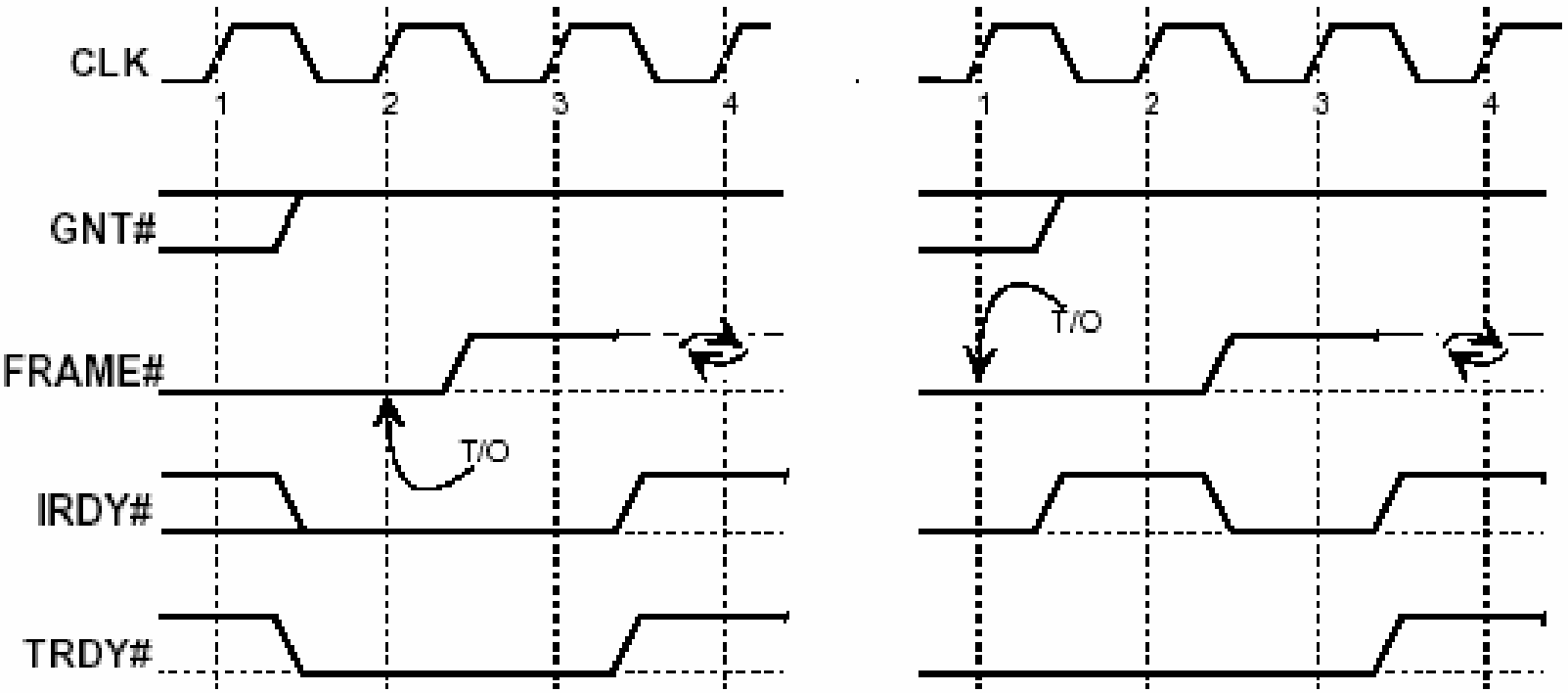
Transaction Termination

- Termination of a PCI transaction may be initiated by either the master or the target.

- Master initiated Termination
  - Completion
  - Timeout
  - Master abort termination
- Target initiated Termination
  - Retry
  - Dissconnect
  - Target-Abort

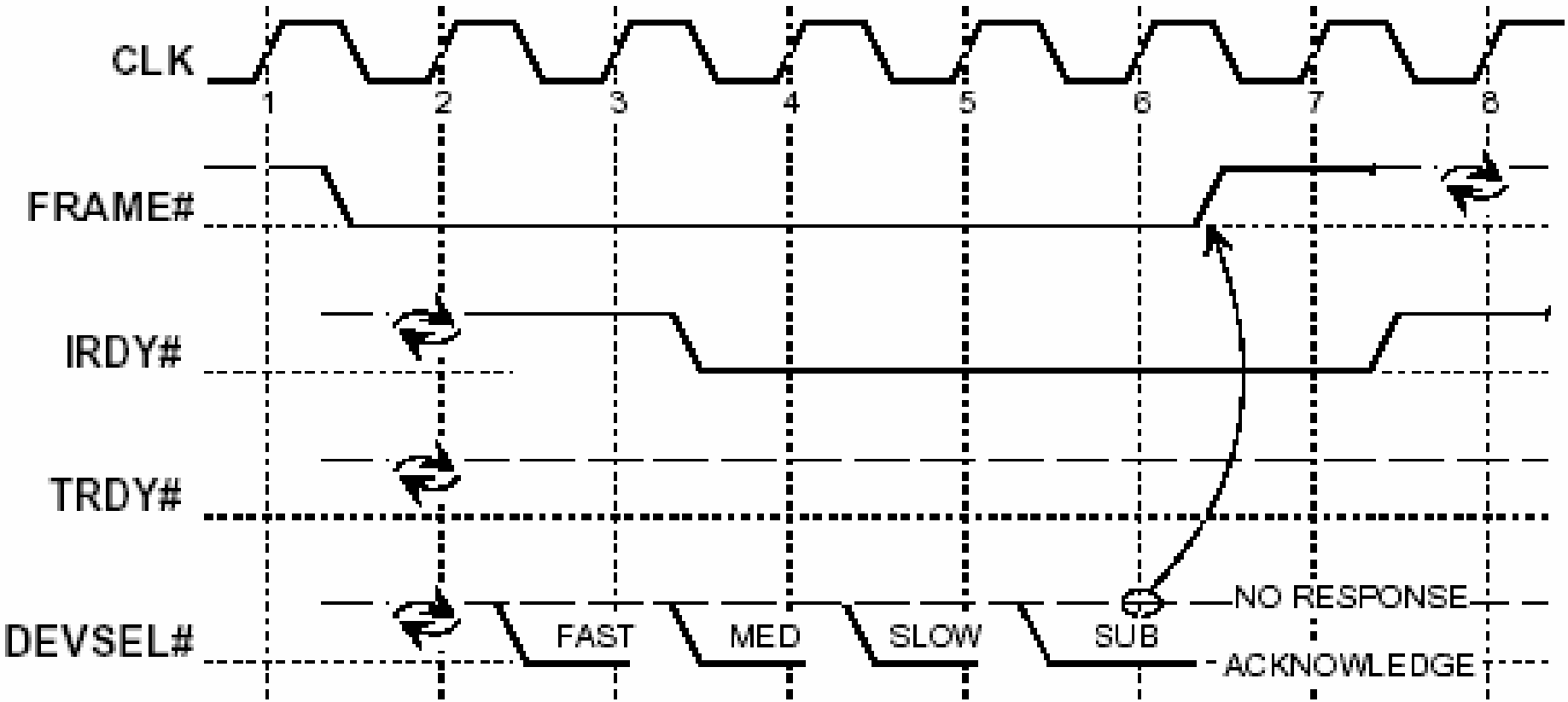
Master Initiated Terminations

- Completion
  - When master has concluded its intendedtransaction
- Timeout
  - When masters GNT# line is deasserted



Master Initiated Terminations

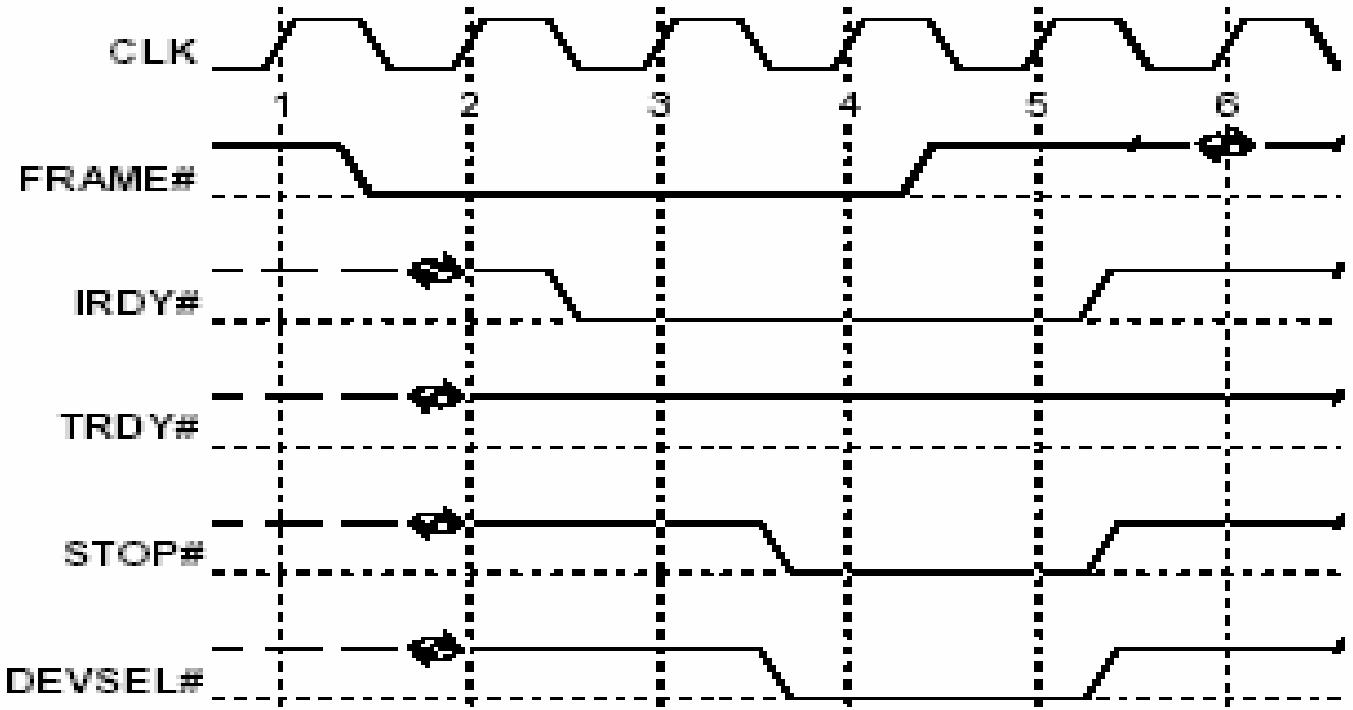
- Master abort termination
  - Occurs when none of the targets asserts the DEVSEL# line to acknowledge the transaction



Target Initiated Terminations

- **Target Retry**

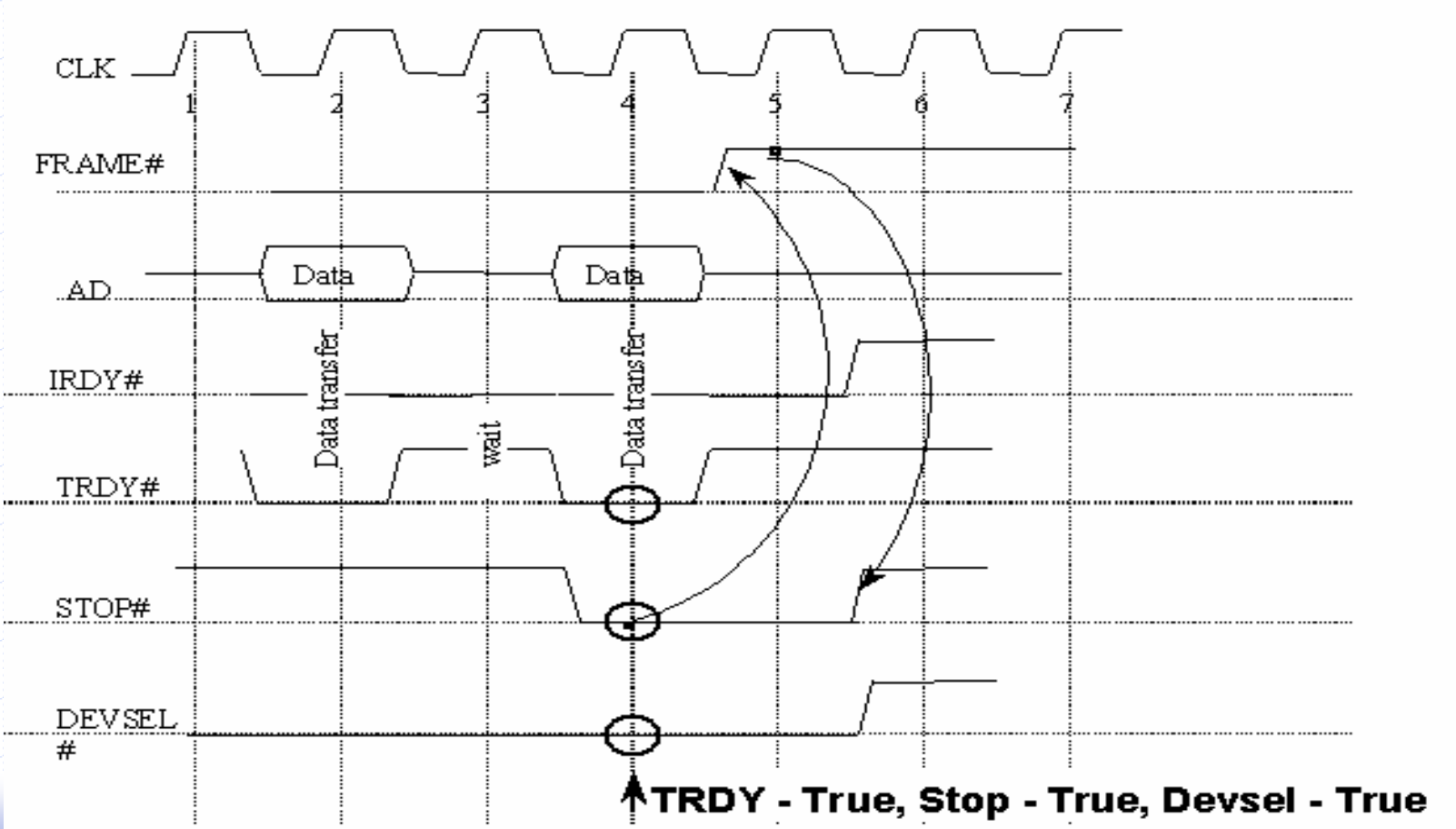
Its the termination requested before any data transfer because the target is busy so it indicates the master to retry later by asserting the Stop# signal.



Target Initiated Terminations

Target Dissconnect

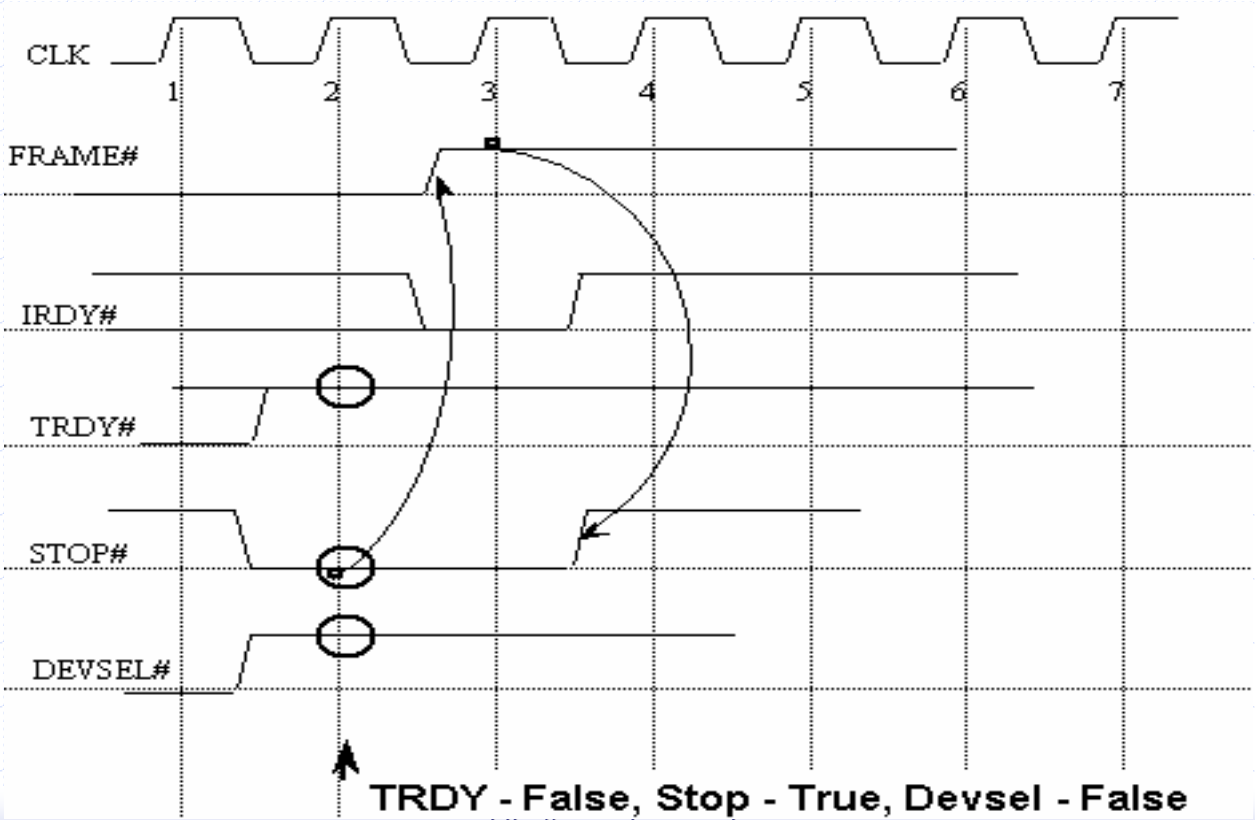
- It is the termination requested when the target is unable to carray out any more transactions. It is signaled by the asserting both the TRDY# and STOP# together during any data phase. It differs from retry, which always occurs on the first data phase.



Target Initiated Terminations

Target-Abort

Its an abnormal termination requested by the target due to the occurance of a fatal error. Once the target has claimed DEVSEL# it can request target-abort at any cycle by deasserting the DEVSEL# and asserting the STOP#.



Why PCI

- High Performance
  - Synchronous bus with operation up to 33 MHz or 66 MHz
- Ease of Use
  - Plug and play configuration support of PCI Local Busadd-in boards
- Longevity
  - Processor independent
  - Support for 64-bit addressing
- Software Compatibility
  - PCI components can be fully compatible with existing driver and applications software.
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